



0.5L PLATFORM
6 LAYERS 143.50MM * 159.07MM

CPU:

AMD FT1 (18w)

System Chipset:

AMD HUDSON-D1 (6w)

On Board Chipset:

**LAN -- RTL8111E
HD Codec -- ALC662-VC1
BIOS -- SPI ROM 32M**

Main Memory:

DDR III X 1 (Max 2GB)

Expansion Slots:

4 IN1 CARD READER

PWM:

Controller -- Intersil ISL6265C

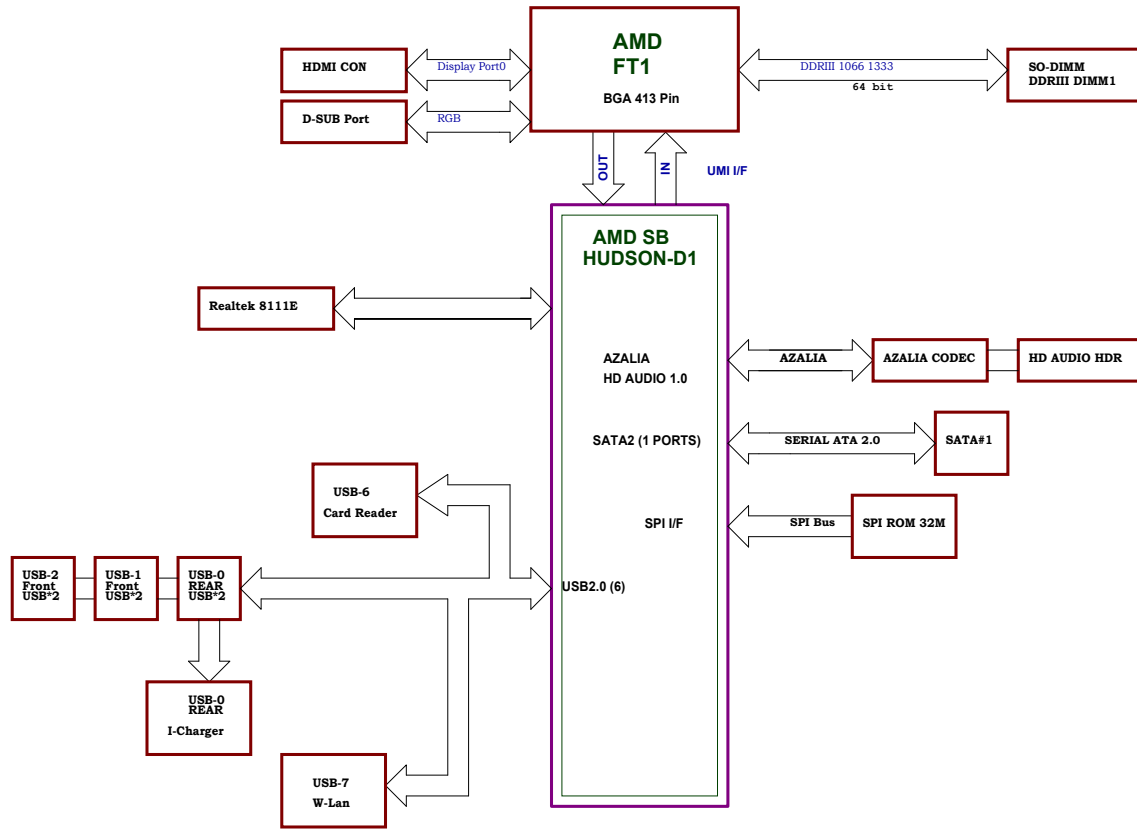
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MS7731-0A Project BLOCK DIAGRAM



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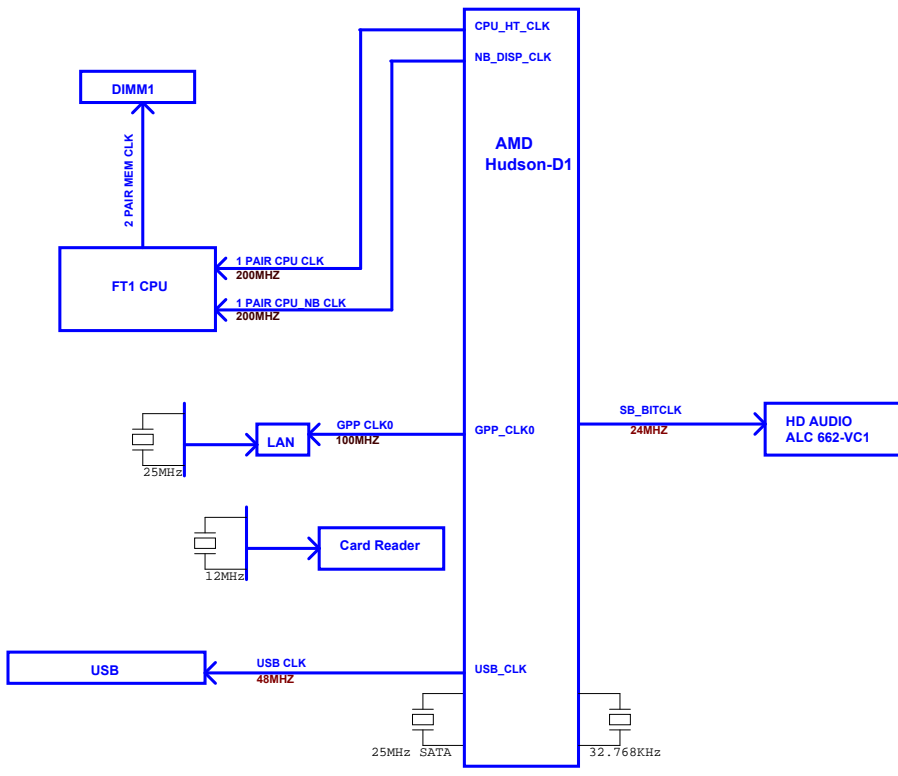
HUDSON-D1

GPIO	Alt Func	I/O/NC	Power	Tolerance	Default	Signal Name
GPIO[23]	PCI Bus Address/Data	I/O	Core	3.3V-5V	GPO	AD23
GPIO[24]	PCI Bus Address/Data	I/O	Core	3.3V-5V	GPO	AD24
GPIO[25]	PCI Bus Address/Data	I/O	Core	3.3V-5V	GPO	AD25
GPIO[26]	PCI Bus Address/Data	I/O	Core	3.3V-5V	GPO	AD26
GPIO[36]	BIF_GEN2_COM PLIANCE_Strap	0	Core	3.3V-5V	GPO	PCI_CLK1
GPIO[37]	BootFailTmrEn	I/O	Core	3.3V-5V	GPO	PCI_CLK2
GPIO[38]	DefaultStrapMode	I/O	Core	3.3V-5V	GPO	PCI_CLK3
GPIO[39]	CPUClkSel	I/O	Core	3.3V-5V	GPO	PCI_CLK4
GPIO[43]	SMBus Clock 0	I/O	Core	3.3V-5V	GPI	HOOD_SW_DET#
GPIO[47]	SMBus Data 0	I/O	Core	3.3V-5V	GPI	SPI_DATAOUT
GPIO[52]	Fan PWM Output 0	I/O	Core	3.3V-5V	GPI	CPU_FAN_PWM
GPIO[53]	Fan PWM Output 1	I/O	Core	3.3V-5V	GPI	HW_DIS
GPIO[56]	Fan Tachometer Input	I/O	Core	3.3V	GPI	CPU_FAN_IN
GPIO[60]	Clock Request# 0	I/O	Core	3.3V-5V	GPI	CLKREQB_LAN
GPIO[67]	Serial ATA Activity Indicator	I/O	Core	3.3V	GPI	SATA_LED
GPIO[162]	SPI Clock	I/O	Resume	3.3V	GPI	SPI_CLK
GPIO[163]	SPI Data Out	I/O	Resume	3.3V	GPI	SPI_DATAOUT
GPIO[164]	SPI Data In	I/O	Resume	3.3V	GPI	SPI_DATAIN
GPIO[165]	SPI Chip Select 1	I/O	Resume	3.3V	GPI	SPI_CS#
GPIO[167]	HD Audio Serial Data	I/O	Resume	3.3V	GPI	AZ_SDATA_IN0
GPIO[171]	Temperature Monitor Input 0	I/O	Resume	3.3V	GPI	THERMDA_CPU
GPIO[172]	Temperature Monitor Input 1	I/O	Resume	3.3V	GPI	USB_PWR_GPIO
GPIO[173]	Temperature Monitor Input 2	I/O	Resume	3.3V	GPI	THRMDA_SB
GPIO[174]	Temperature Monitor Input 3	I/O	Resume	3.3V	GPI	TALERT#
GPIO[175]	Voltage Monitor Input 0	I/O	Resume	3.3V	GPI	LED_VSB
GPIO[176]	Voltage Monitor Input 1	I/O	Resume	3.3V	GPI	LED_VCC
GPIO[177]	Voltage Monitor Input 2	I/O	Resume	3.3V	GPI	CHARGE_S0
GPIO[178]	Voltage Monitor Input 3	I/O	Resume	3.3V	GPI	CHARGE_S1
GPIO[179]	Voltage Monitor Input 4	I/O	Resume	3.3V	GPI	LAN_ISOLATEB
GPIO[195]	SMBus Clock 3 for CPU TSI	I/O	Resume	3.3V	GPI	AMD_SID
GPIO[196]	SMBus Data 3 for CPU TSI	I/O	Resume	3.3V	GPI	AMD_SID
GPIO[199]	EC_PWM2	I/O	Resume	3.3V	GPI	EC_PWM2

DDR-III SO-DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM1	00	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1

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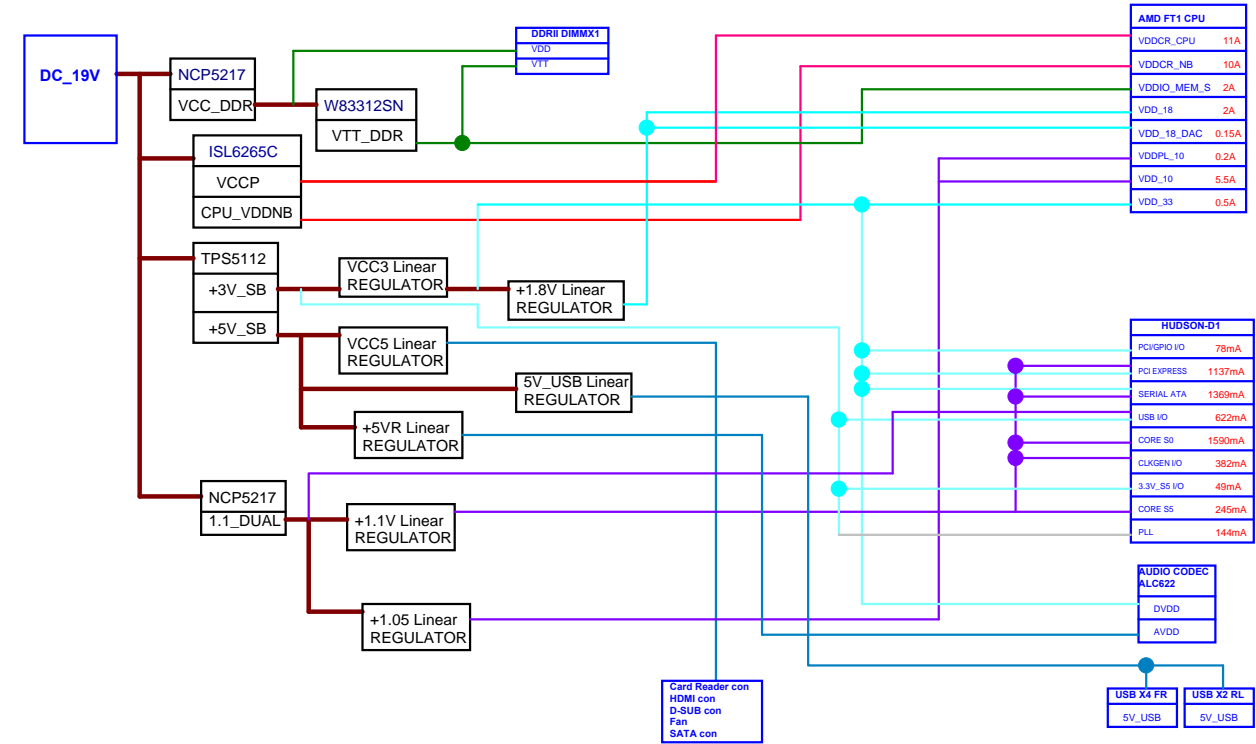


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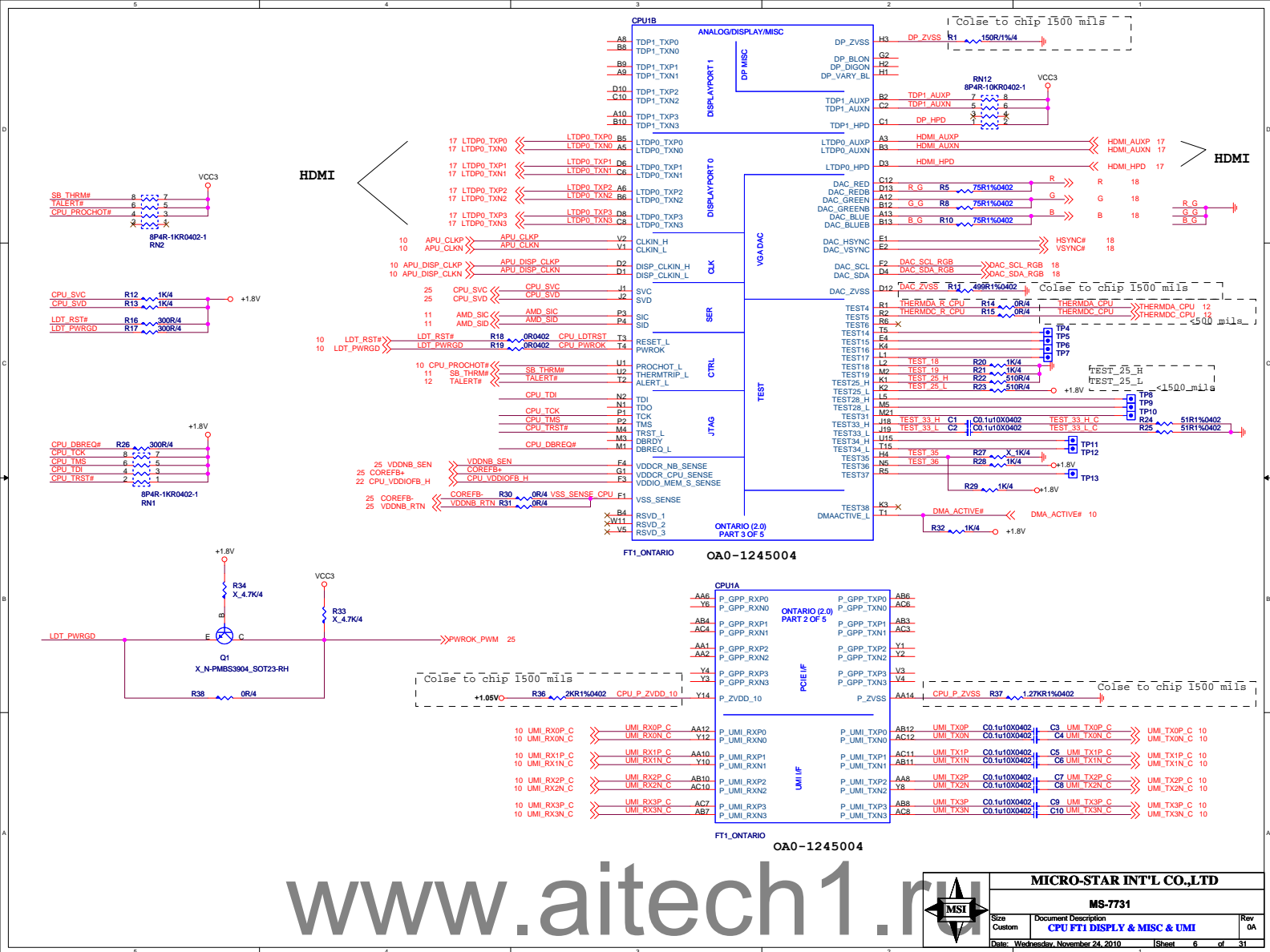


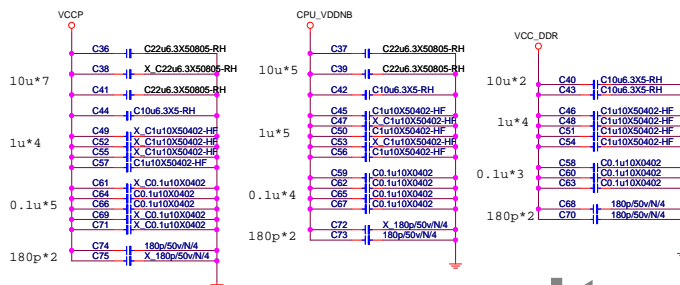
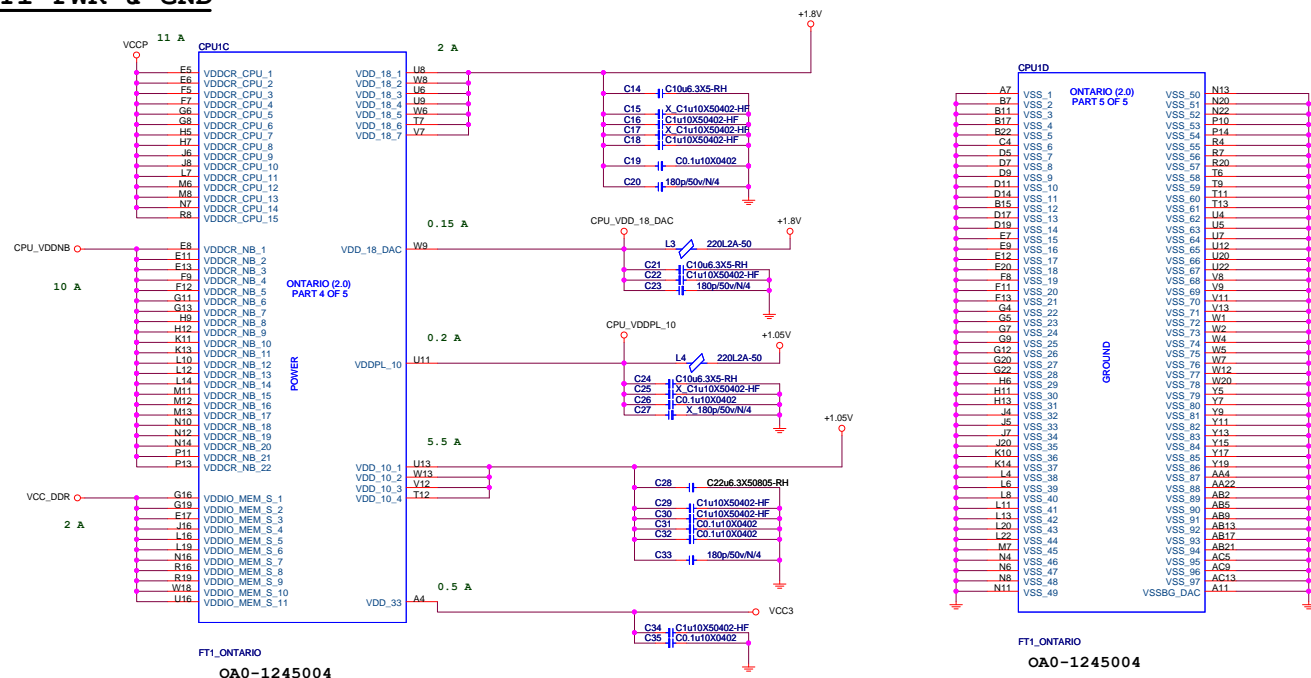
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Power Deliver Chart



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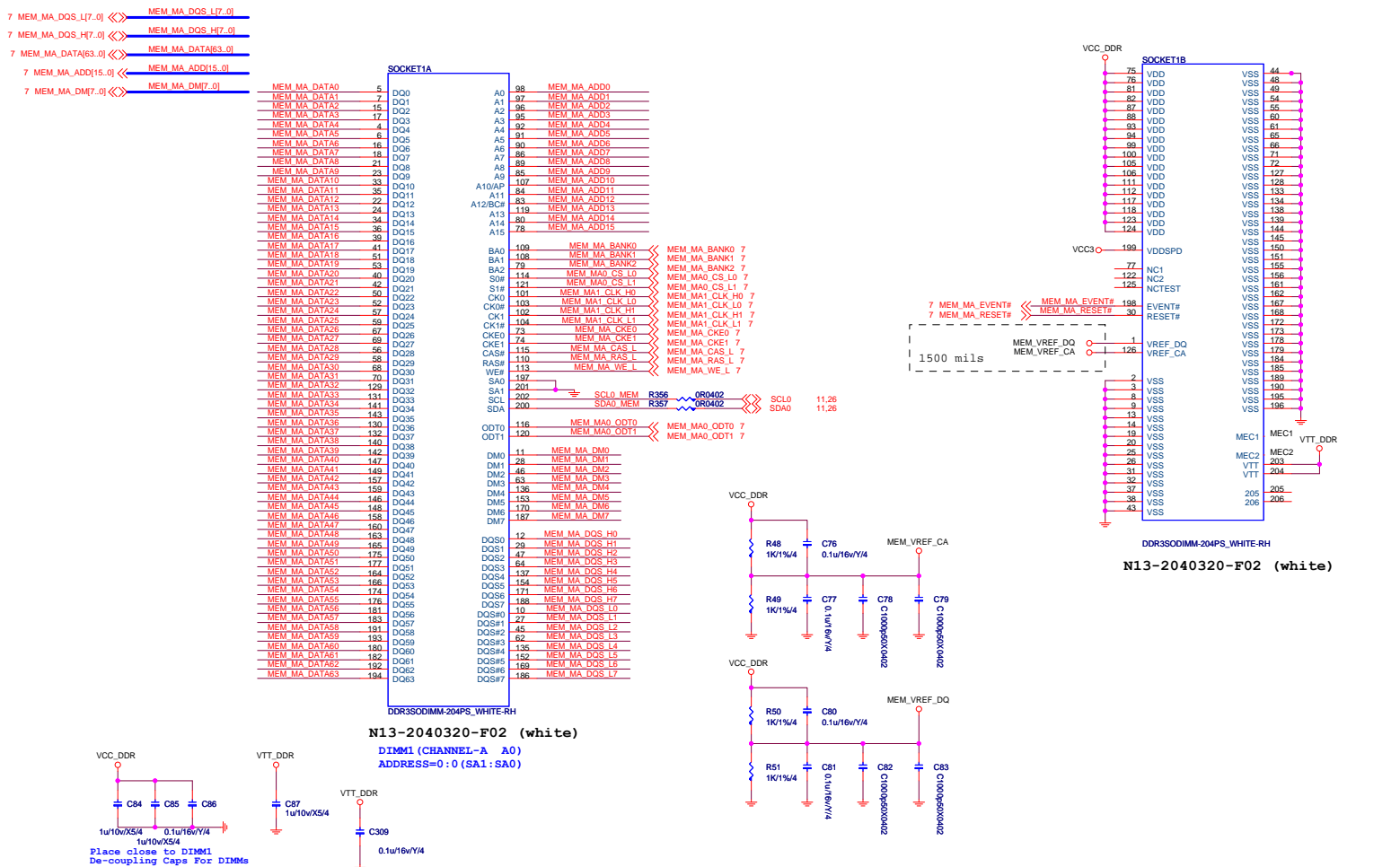




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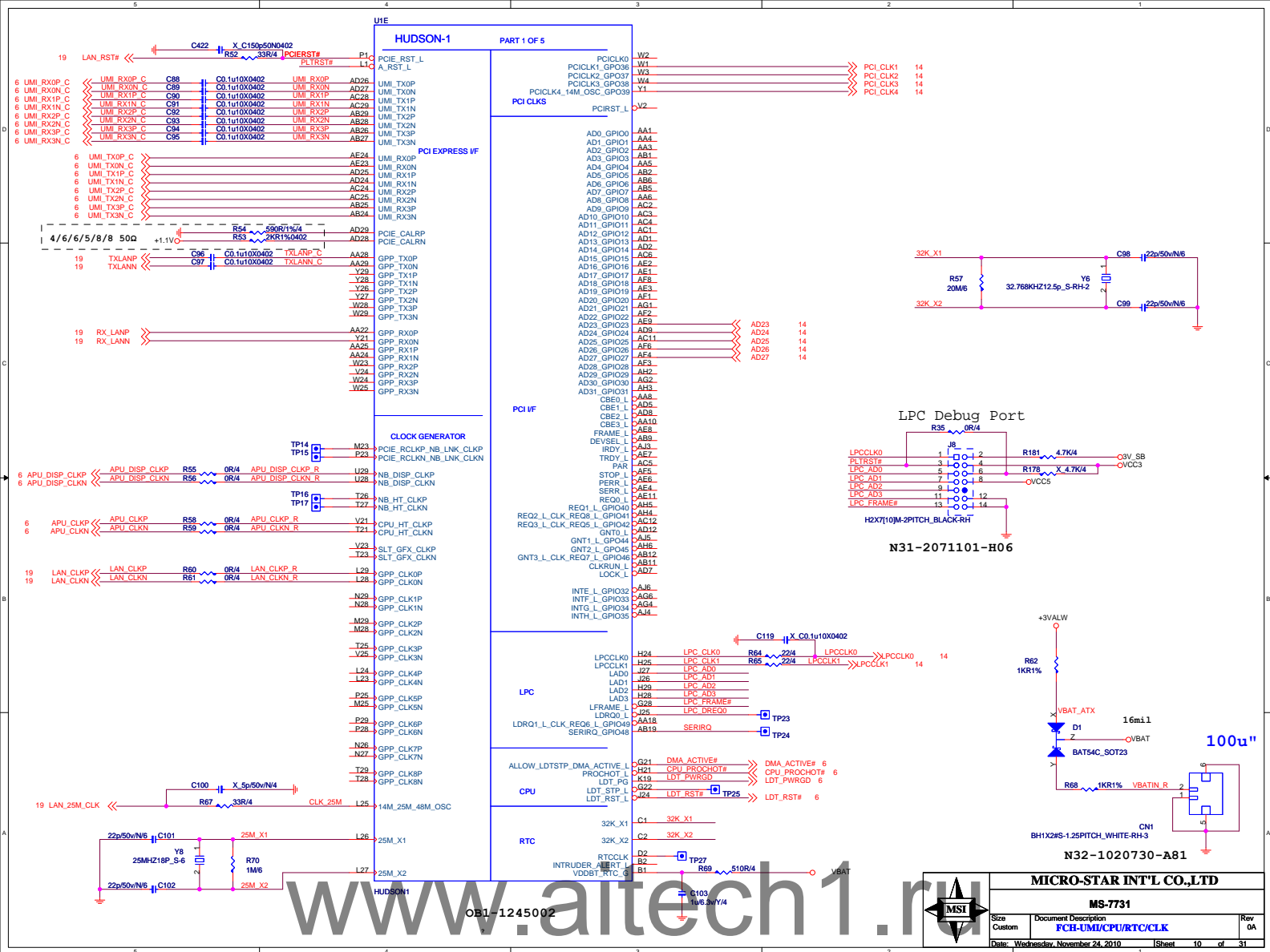
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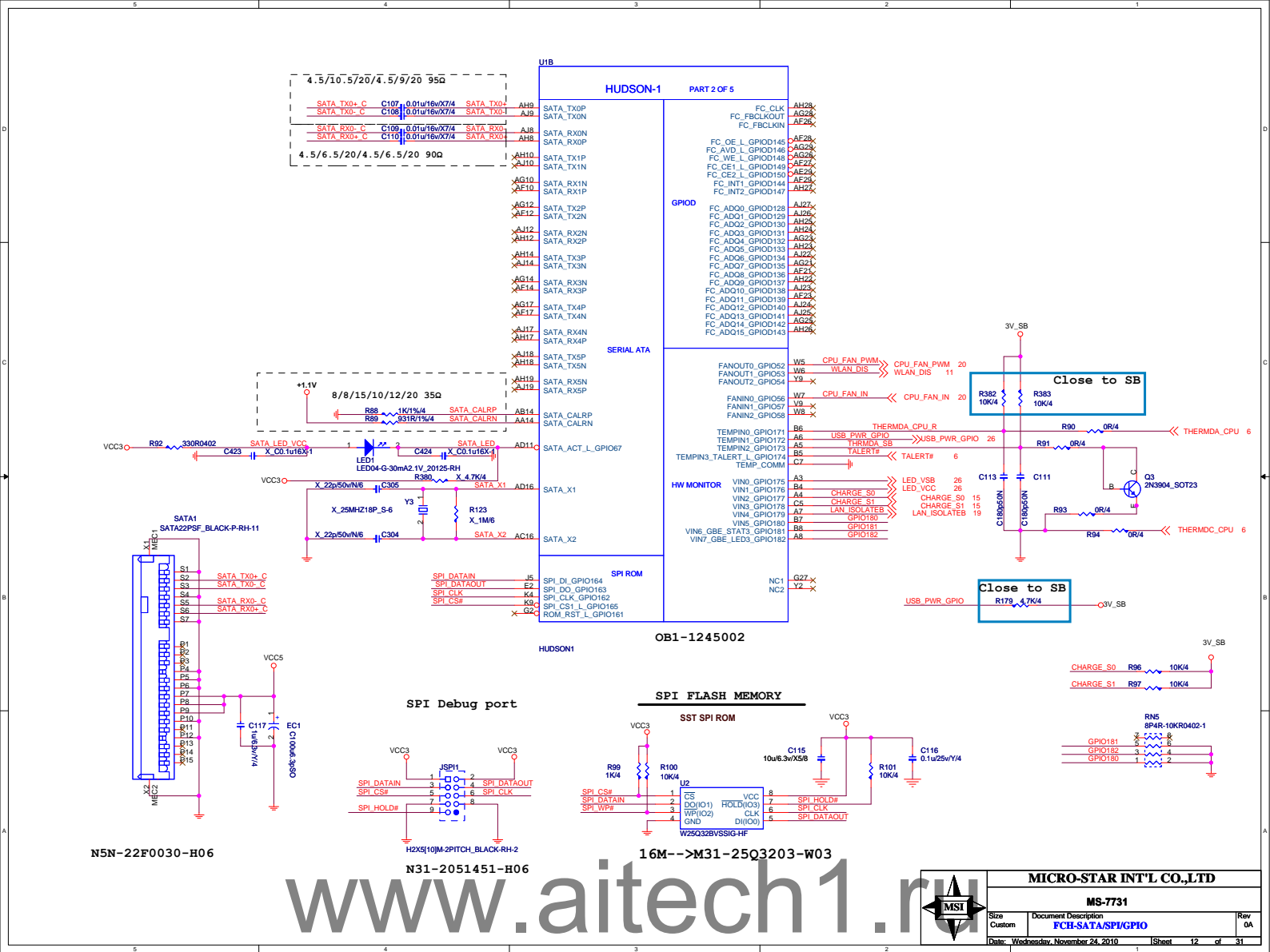


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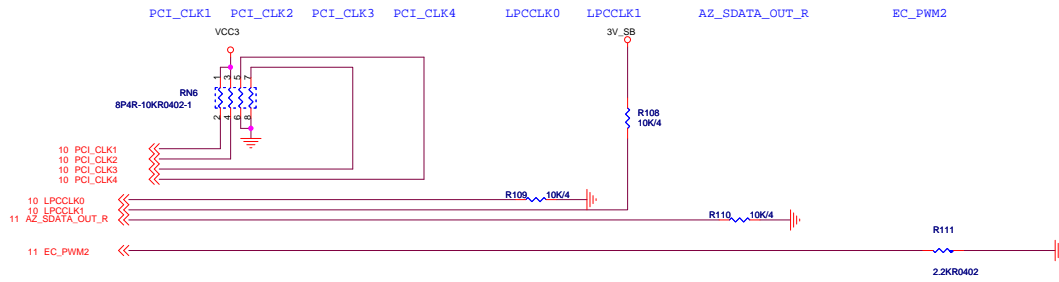
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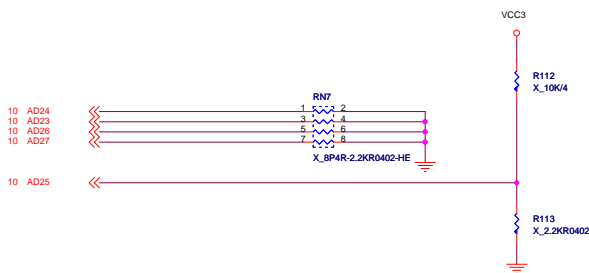




REQUIRED STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDATA_OUT_R	EC_PWM3/EC_PWM2
PULL HIGH	PCIE GEN2 DEFAULT	WatchDog Enable DEFAULT	Debug Straps Enable	CPUClkSel Disable	EC ENABLE	CLKGEN ENABLED DEFAULT	Reserved (as low power mode is not supported)	ROM TYPE: 10 = SPI ROM DEFAULT
PULL LOW	PCIE GEN1	WatchDog Disable	Debug Straps Disable DEFAULT	Internal CLK-GEN DEFAULT	EC DISABLE DEFAULT	CLKGEN DISABLED	Required settling (performance mode) DEFAULT	ROM TYPE: 01 = LPC ROM



FCH DEBUG STRAPS

INTERNAL Pull-Up FOR PCI_AD[23/24/26/27]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DEFAULT	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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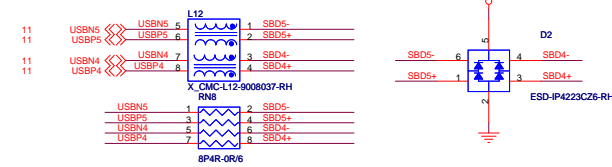


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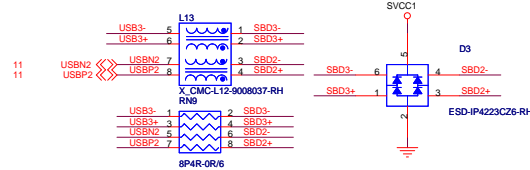
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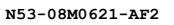
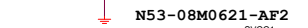
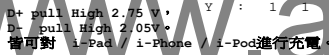
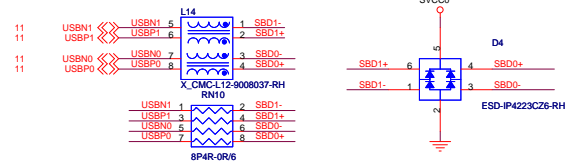
Trace lengths must be less 12 inches



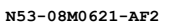
Trace lengths must be less 12 inches



Trace lengths must be less 12 inches

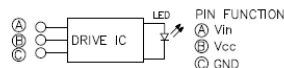
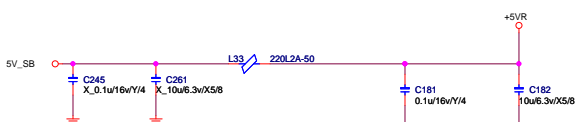
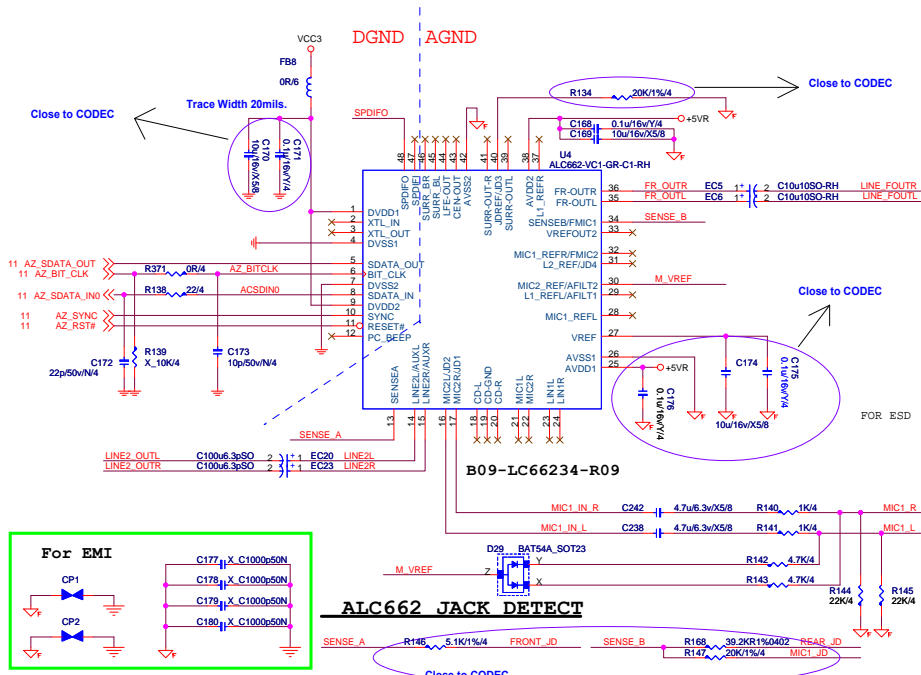


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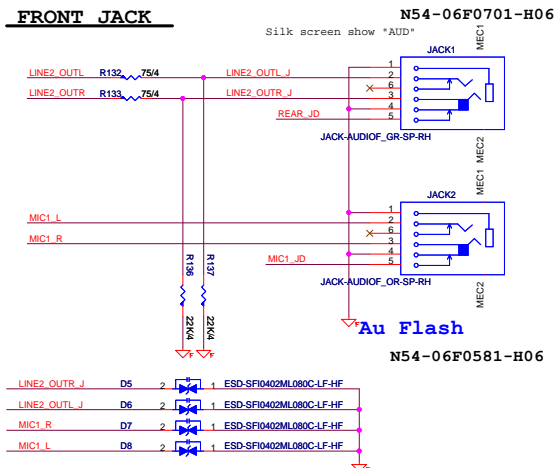


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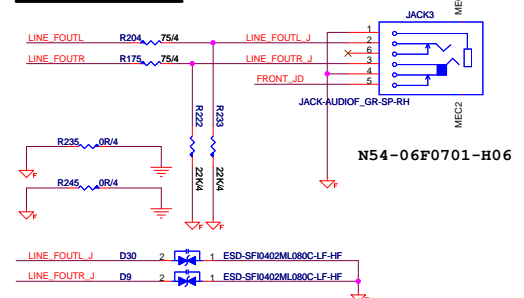
ALC662 CODEC



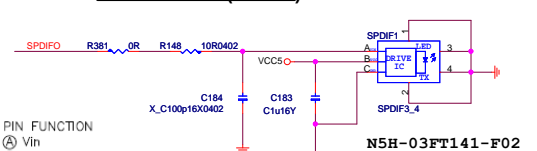
FRONT JACK



REAR JACK



SPDIF_OUT (REAR)



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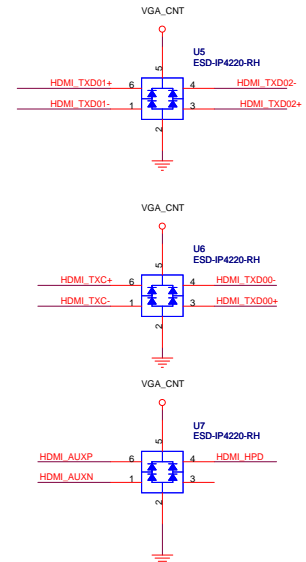
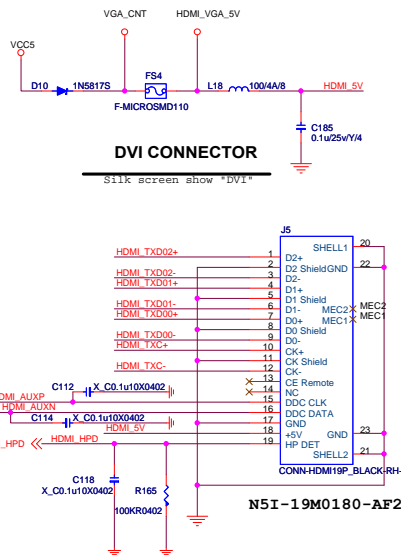
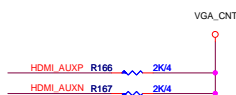
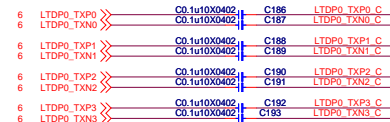
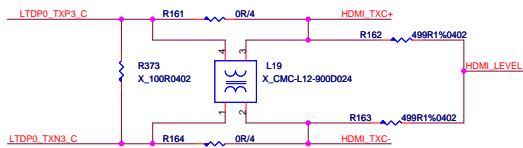
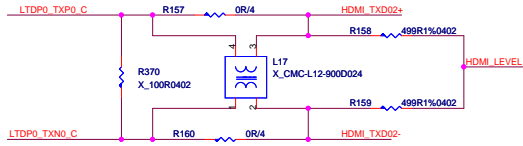
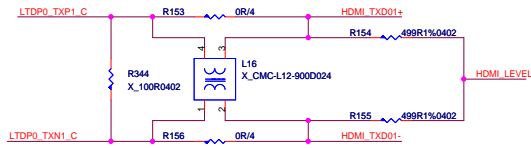
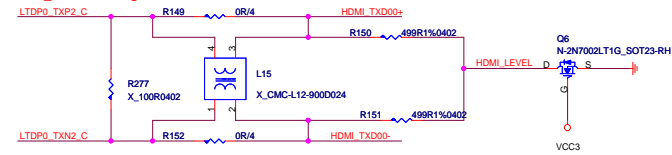
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Table 49. DisplayPort Configurations

Interface	DisplayPort Configurations						
	LTDPO x4 or TDP1 x4				DP Aux +	DP Aux -	HPD
	3	2	1	0			
DP Only	MainLink[3:0]				AUX ¹		HPD
DP++ (use LTDPO or TDP1)	MainLink[3:0]				AUX ¹		HPD
DVI	Channel Clock	Ch 2	Ch 1	Ch 0	DDC ² Clock	DDC ² Data	-
HDMI™	Channel Clock	Ch 0	Ch 1	Ch 2	DDC ² Clock	DDC ² Data	Cable Detect
LVDS Panel (use LTDPO)	Channel Clock	Ch 2	Ch 1	Ch 0	DDC ² Clock	DDC ² Data	-
eDP Panel (use LTDPO or TDP1)	ML3	ML2	ML1	ML0	AUX ¹		HPD
							Inverter Power LCD Logic Power Inverter Control
							Inverter Power LCD Logic Power Inverter Control

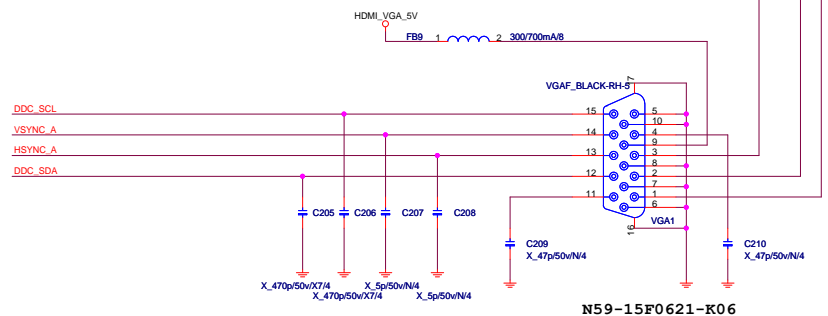
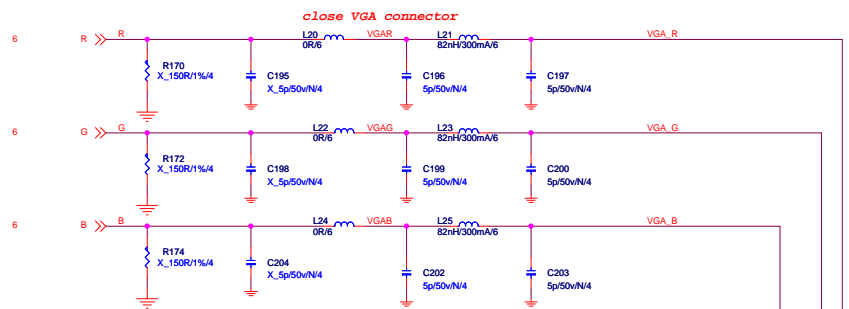
1. Auxiliary Mode, AC coupled (see Table 50 on page 116)

2. I²C Mode, DC coupled

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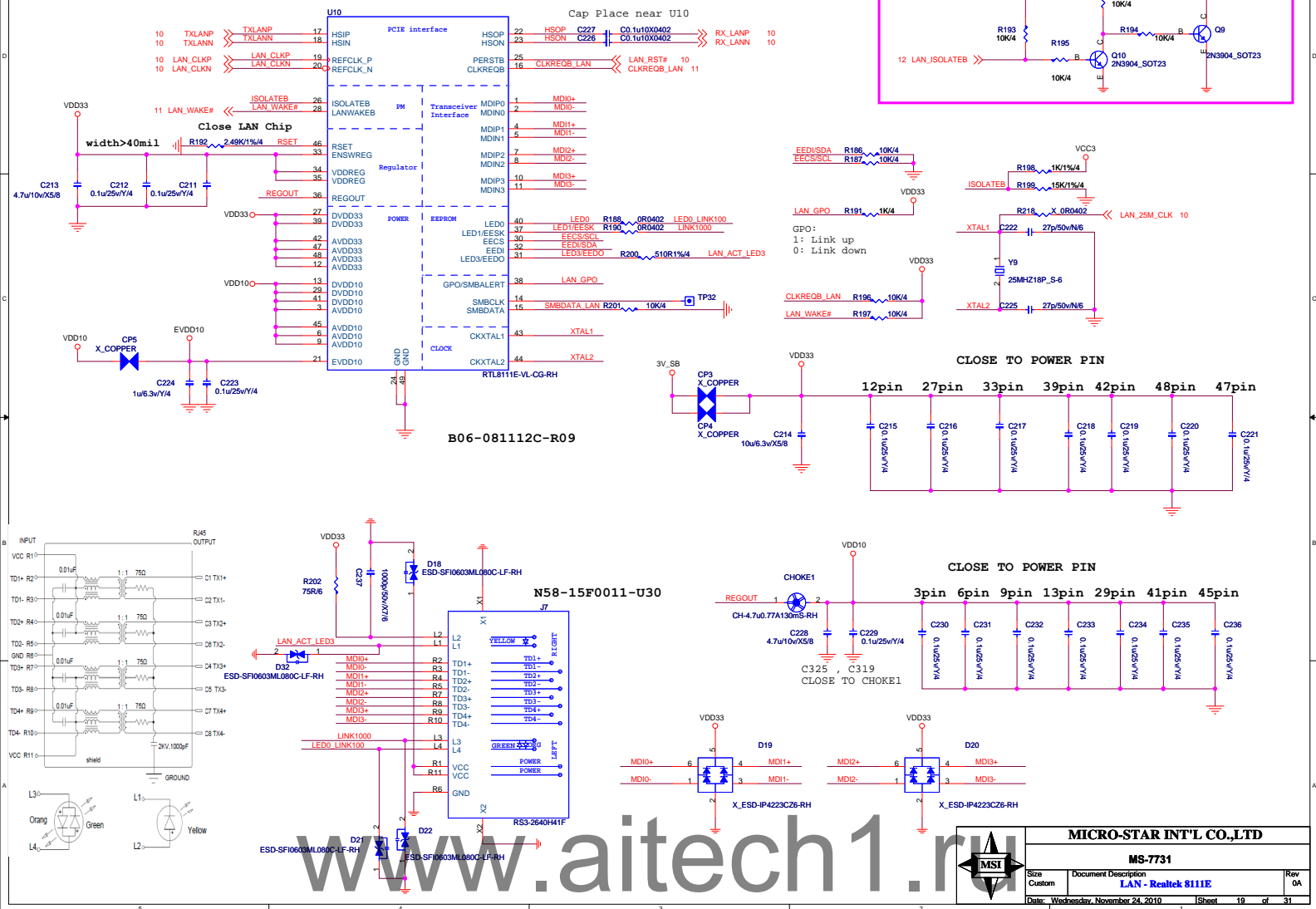


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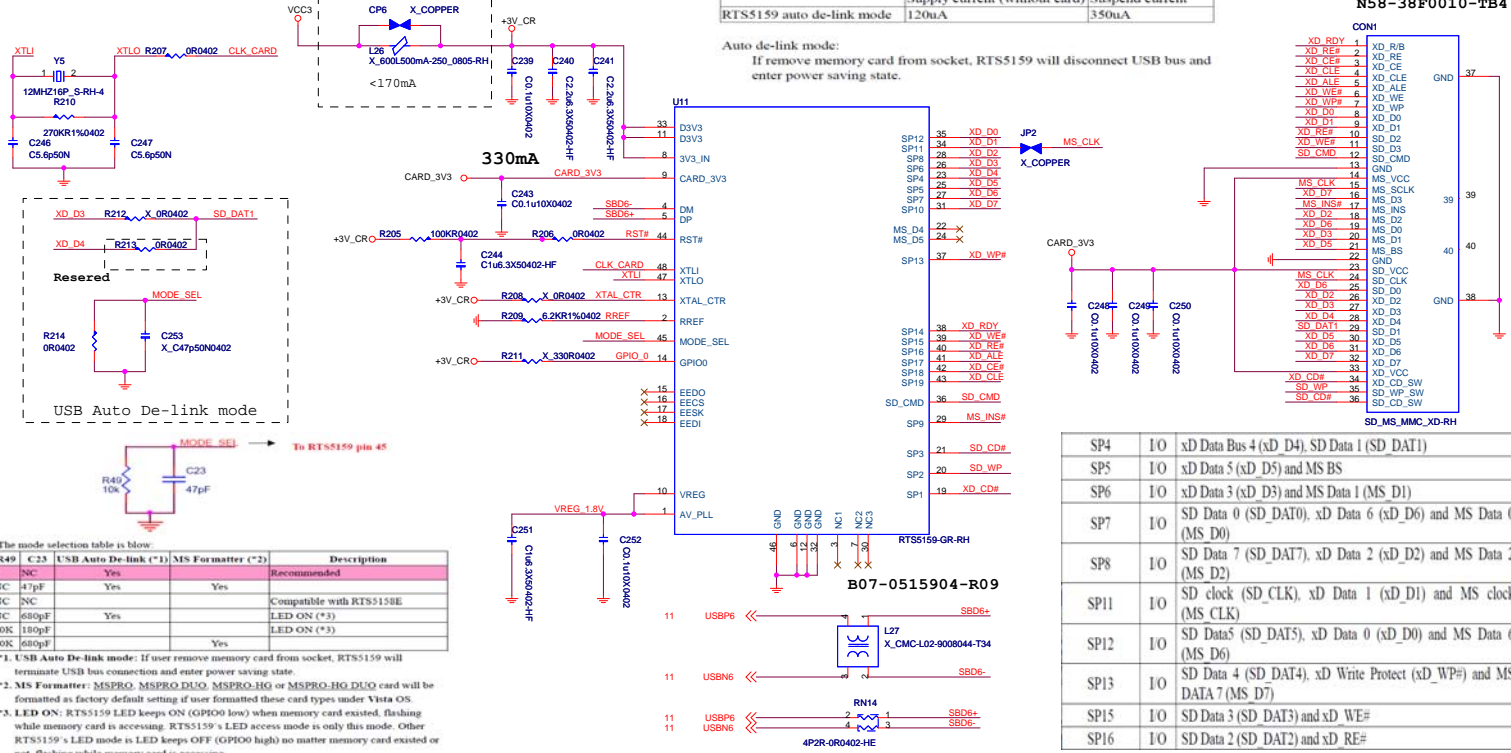


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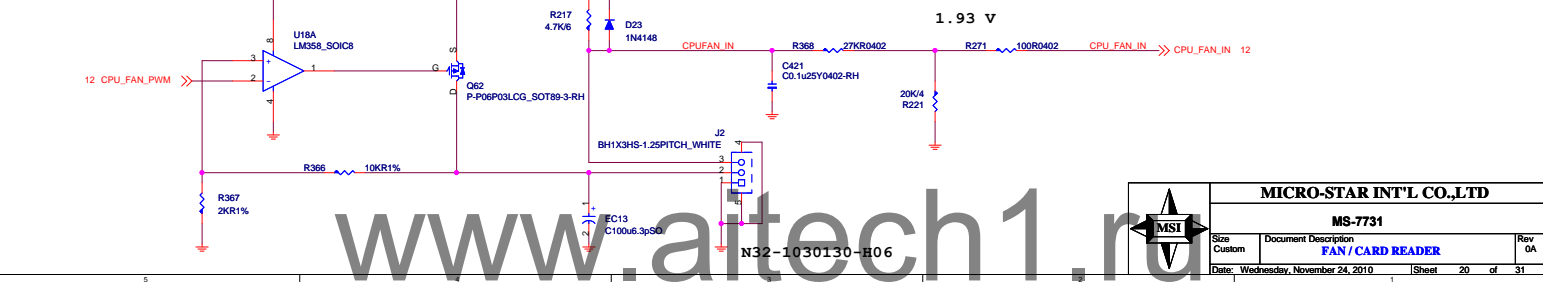
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RTL8111E

Card Reader



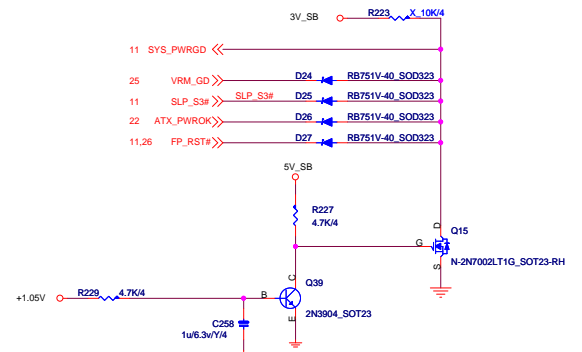
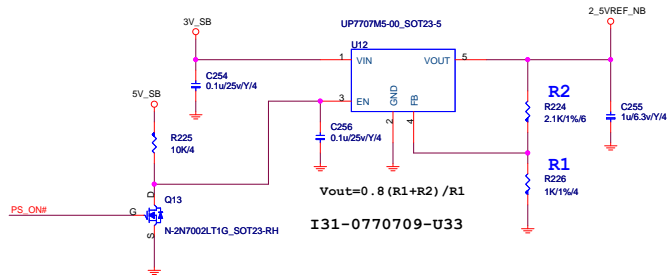
FAN CONTROL



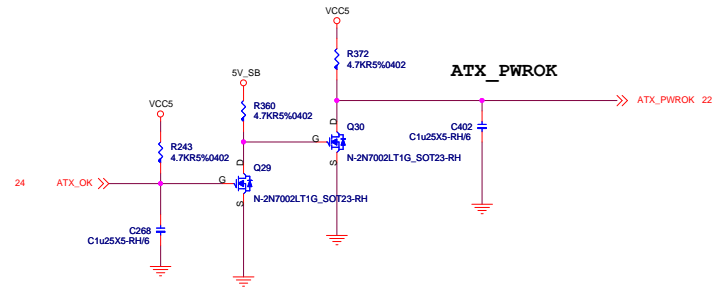
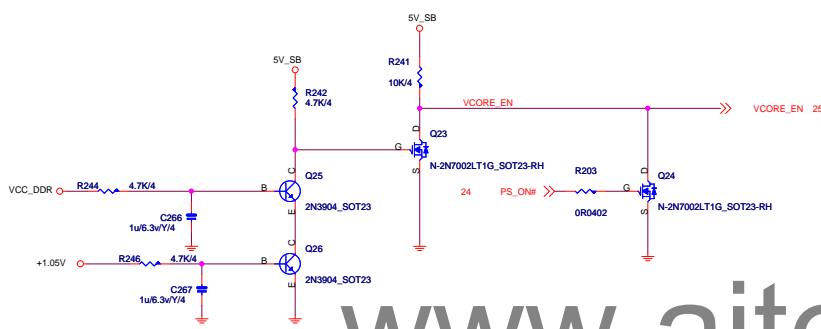
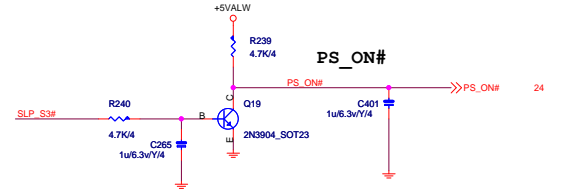
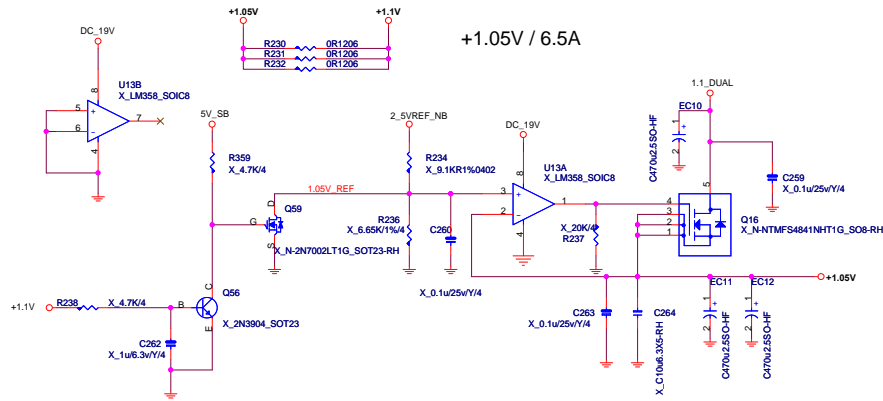
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2_5VREF_NB



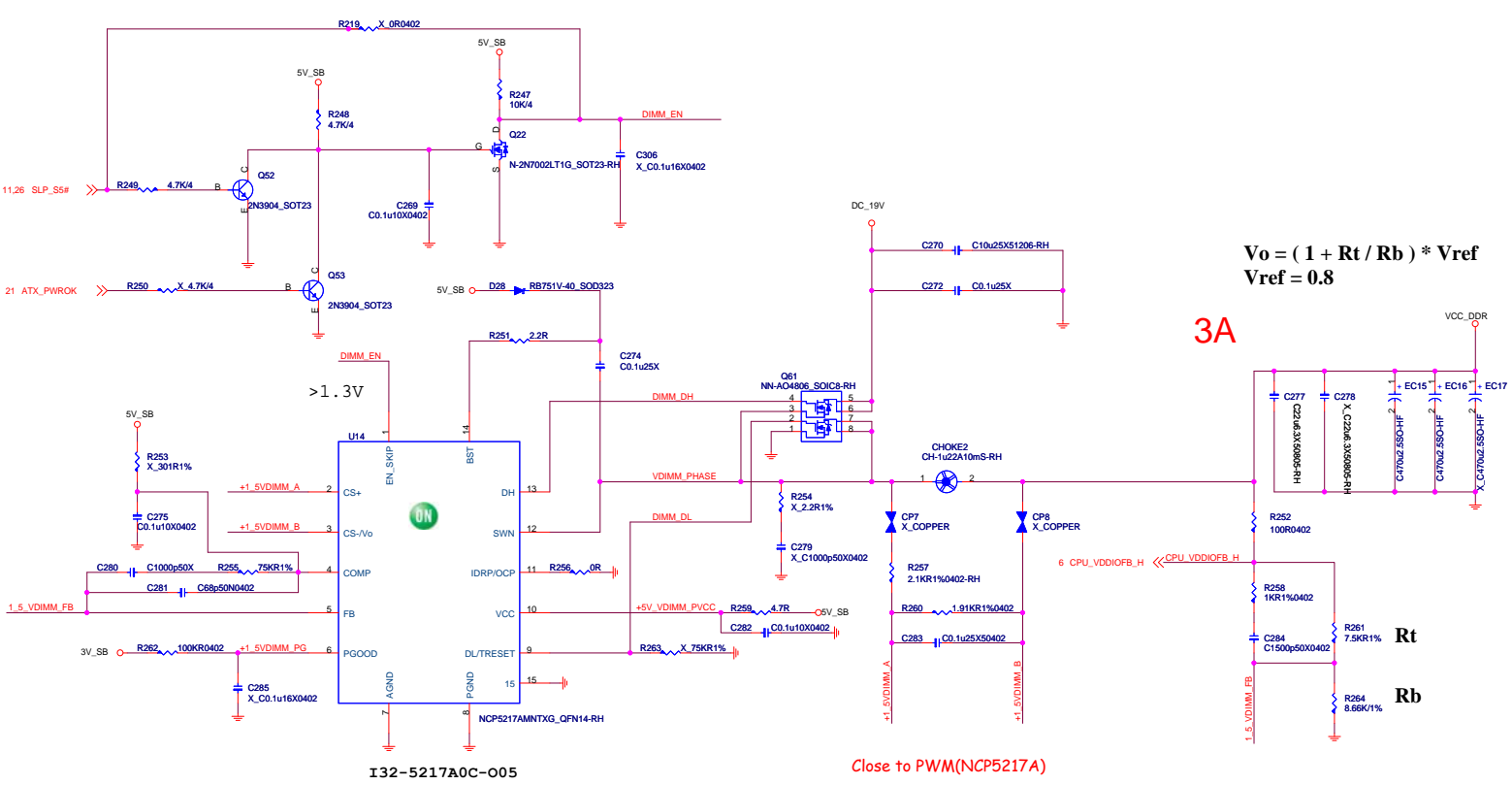
+1.05V / 6.5A



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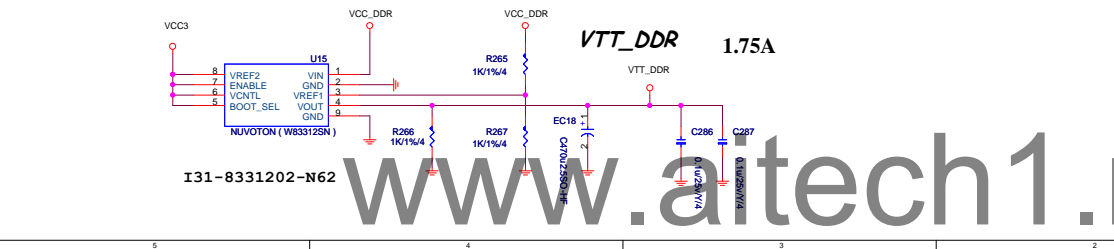


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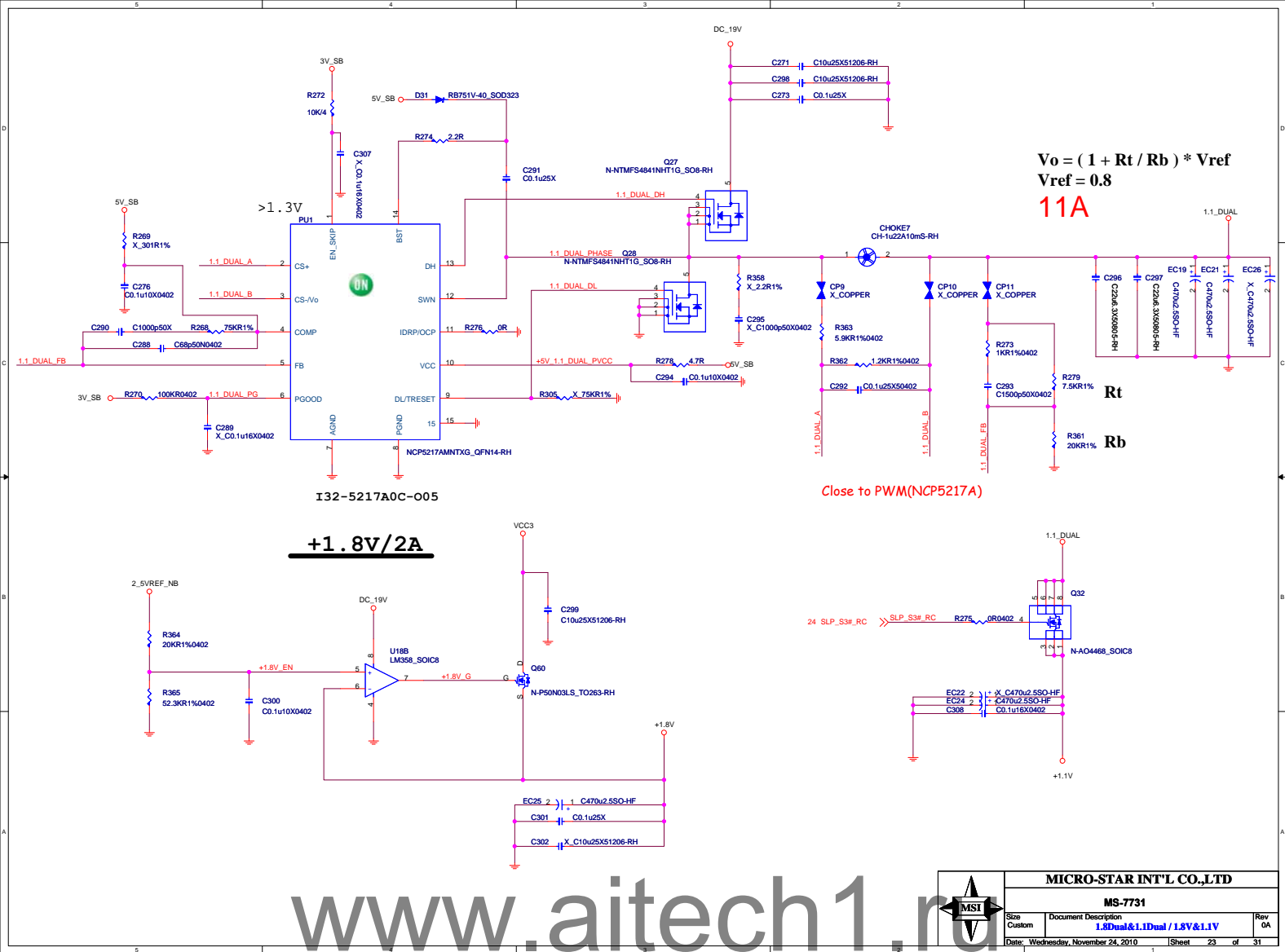


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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USB POWER

DC 19V

5V_SB

R352 10K/4

R351 10K/4

USB_PWRSW

Q57

Q58

2N3904_SOT23

2N3904_SOT23

GPIO17

12 USB_PWR_GPIO

R354

4.7K/4

Q54

N-NTMFS4841NH1T1G_S08-RH

5V_SB

USB_PWRSW

5V_USB

C381

0.1uF/50V/K

EC41

C470A2_S08-HF

C396 C0.1u25X

C387 C0.1u25X

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Document Description

ATX/Front Panel/USB pow

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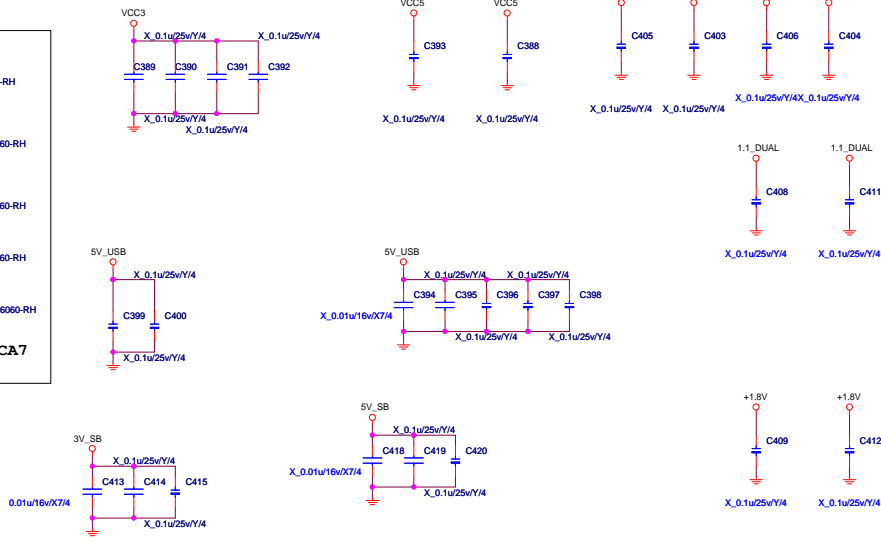
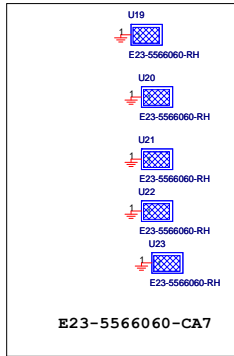
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Rev 0A

	Single color LED		Dual color LED	
	LED1	LED_SW	LED1	LED_SW
S0	H	L	H	L
S1/S3	Blinking	L	L	H
S4/S5	L	L	L	L



EMI solution

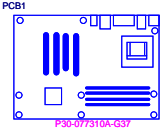


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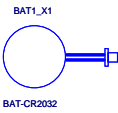


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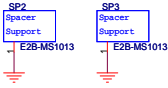
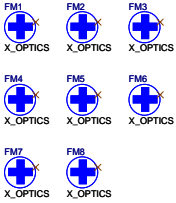
PCB



PCB : 1080
P30-077310A-G37
P30-077310A-E55

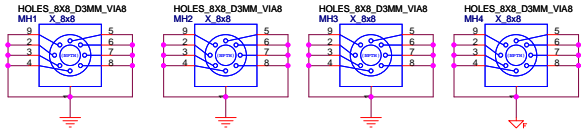


Optics Orientation Holes



E2B-1013010-L63

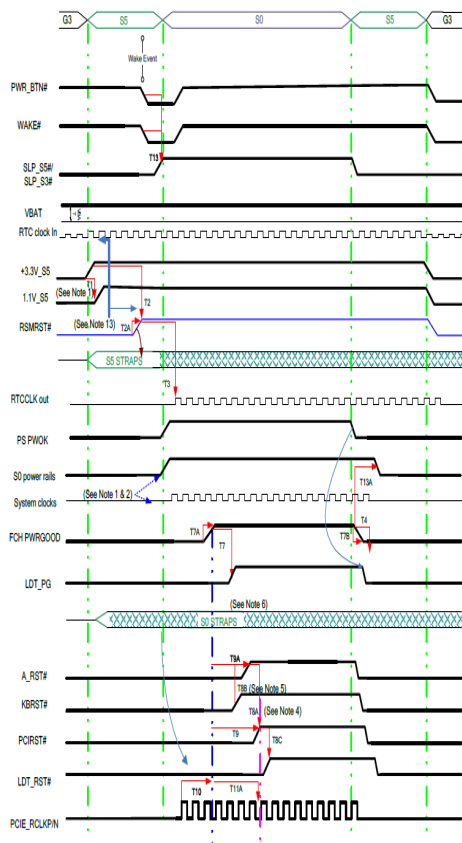
Mounting Holes



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Chapter 5 Power Rail Power-Up Sequence

The Hudson-1 power rail power-up sequence is shown below. In general, the requirement is that lower voltages must never exceed higher voltages during power up.

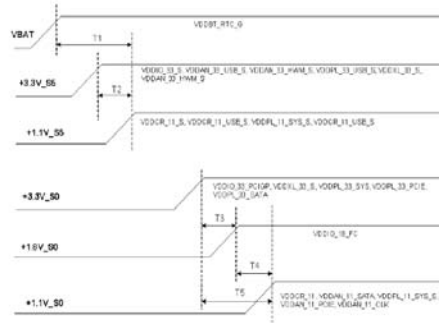
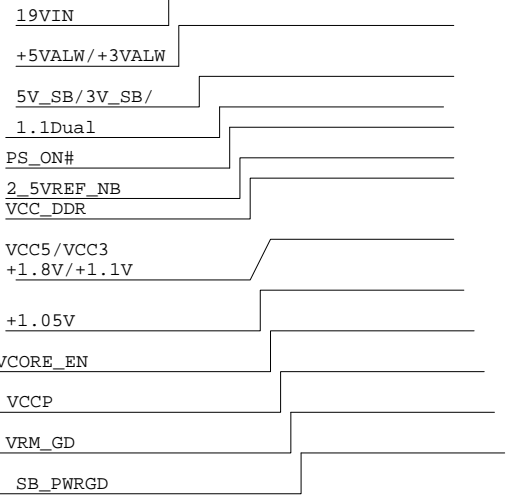


Figure 47 FCH Power Rail Power-Up Sequence



CPU Power sequence

Table 32. Power Sequencing Group Definitions

Power Group A	Power Group B
VDD_10	VDDCR_CPU
VDDPL_10	VDDCR_NB
VDD_18	
VDD_18_DAC	
VDDIO_MEM_S	
VDD_33	

8.1.1 PWROK Sequencing Requirements

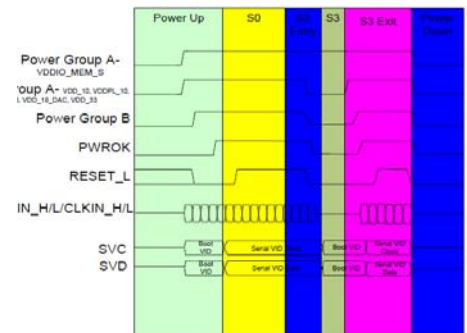


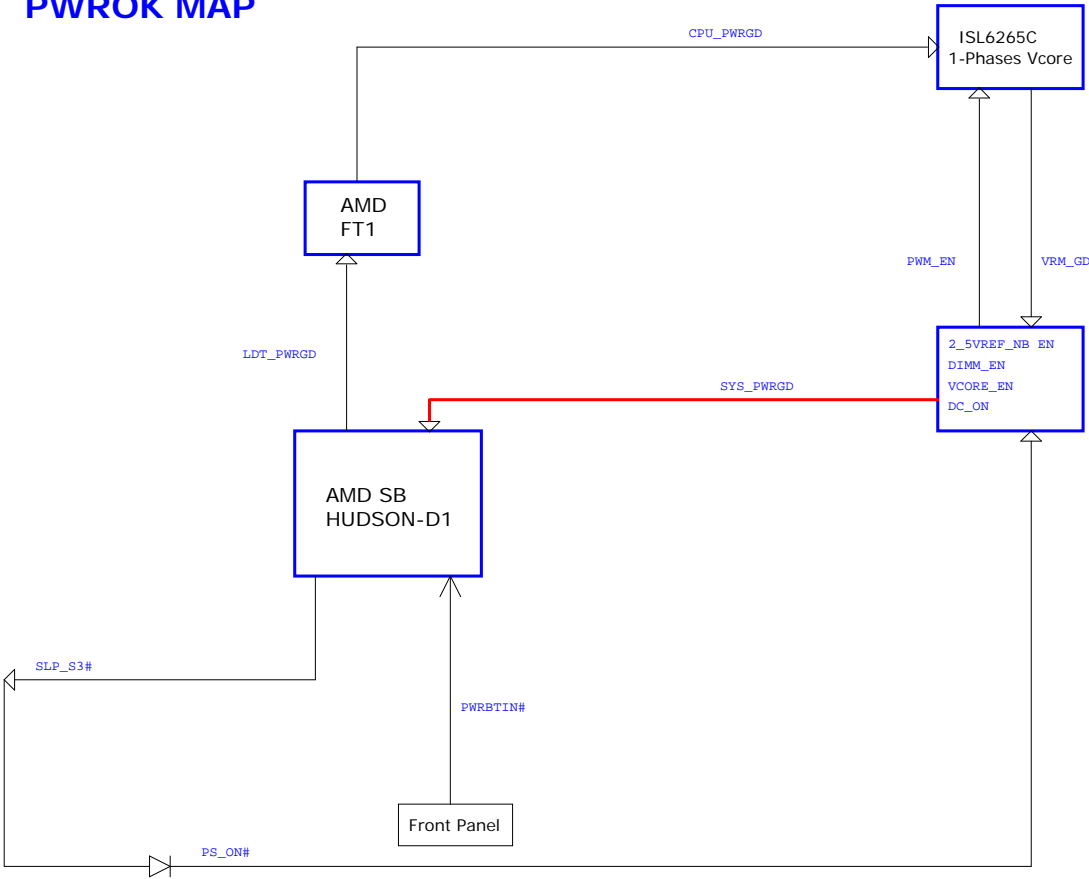
Figure 6. Power Sequencing with S3 detail

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PWROK MAP



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Page30: stuff D48-57 audio ESD diode

Page12.14: change bom XMM1 XMM2 color from white to blue

Page29: empty RN17 20 28 and stuff L12 13 21 for mei

0211

Page40: add bumper